(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 822 586 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
04.02.1998 Bulletin 1998/06

(51) Int Cl.[6]: **H01L 21/316**, H01L 21/76, H01L 21/768, H01L 23/48

(21) Application number: **97305711.0**

(22) Date of filing: **30.07.1997**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **30.07.1996 US 23133 P**

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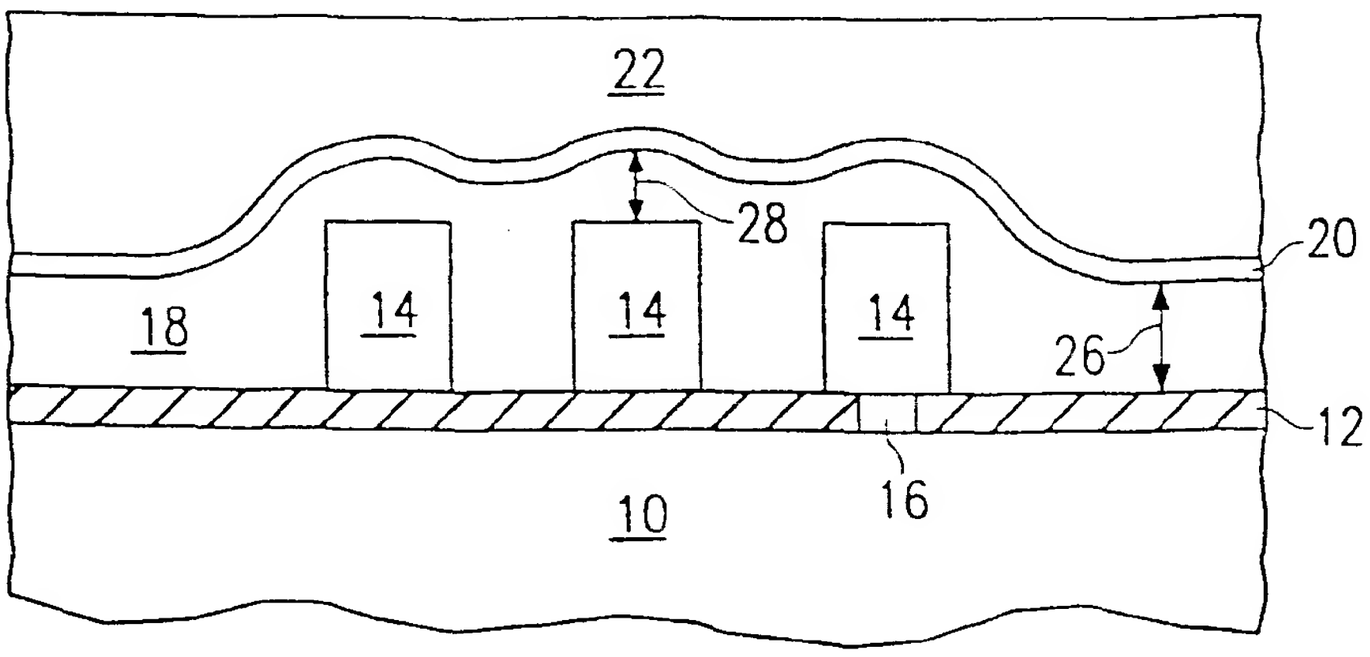
(54) Improvements in or relating to integrated circuits

(57) An improved method is provided for integrating HSQ into integrated circuit structures and processes, especially those requiring multiple levels of interconnect lines. In a preferred embodiment, interconnect lines 14 are first patterned and etched on a substrate 10. A low-k material such as hydrogen silsesquioxane (HSQ) 18 is spun across the surface of the wafer to fill areas between interconnect lines. A capping layer such as SiO_2 20 is applied to on top of the low-k material. The HSQ is then heated to cure. A thick SiO_2 planarization layer 22 may then be applied and planarized. In other embodiments, the HSQ and SiO_2 process steps can be repeated for multiple layers of HSQ.

FIG. 1



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Description

FIELD OF THE INVENTION

This invention generally relates to integrated circuits, and more particularly to methods and structures for reducing capacitance in integrated circuits such as between closely spaced interconnect lines or in silicon trench isolation. In a particular example, the invention relates to a method of suppressing cracks during cure of Hydrogen Silsesquioxane's (HSQ) thin films to obtain an immunity to high temperature processes and increase the porosity and reduce the dielectric constant of the HSQ.

BACKGROUND OF THE INVENTION

Integrated circuits increasingly require very close spacing of interconnect lines and many now require multiple levels of metalization, as many as seven, to interconnect the various circuits on the device. Since closer spacing increases capacitance between adjacent lines, as the device geometries shrink and densities increase, capacitance and cross talk between adjacent lines becomes more of a problem. Therefore, it becomes increasingly more desirable to use materials with lower dielectric constants to offset this trend and thereby lower capacitance between closely spaced interconnects.

Interconnect capacitance is a distributed quantity in the metalization, however, two components dominate: the line-to-substrate, or line-to-ground capacitance and line-to-line capacitance. For ultra large scale integration at 0.25 micron design rules and beyond, performance is dominated by interconnect RC delay, with line-to-line capacitance being the dominant contributor to total capacitance. For example, theoretical modeling has shown that when the width/spacing is scaled down below 0.3 micron, the interlayer capacitance is so small that total capacitance is dictated by the line-to-line capacitance, which constitutes more than 90% of the total interconnect capacitance. Therefore, a reduction of the line-to-line capacitance alone will provide a dramatic reduction in total capacitance.

The intermetal dielectric (IMD) of the prior art is typically SiO_2 which has a dielectric constant of about 4.0. It would be desirable to replace this material with a material having a lower dielectric constant. As used herein, low dielectric constant or low-k means a material having a dielectric constant of lower than about 3.5 and preferably lower than 3 and most preferably about 2 or lower. Unfortunately, materials having a lower dielectric constant have characteristics that make them difficult to integrate into existing integrated circuit structures and processes. Many polymeric materials such as polysilsesquioxane, parylene, polyimide, benzocyclobutene and amorphous Teflon have lower dielectric constants (lower permittivities). Other preferred materials are Aerogel or Xerogel which are typically made from a gelation of tetraethoxysilane (TEOS) stock solution. Compared to SiO_2, these preferred low-k materials typically have low mechanical strength, poor dimensional stability, poor temperature stability, high moisture absorption and permeation, poor adhesion, large thermal expansion coefficient and an unstable stress level. Because of these attributes, the use of polymer or other low dielectric materials as a stand alone replacement for SiO_2 in integrated circuit processes or structures is very problematic.

An earlier United States Patent application, by applicant herein, SN 60/013,866 disclosed a method and structure for integrating HSQ and other low dielectric constant materials. This application discloses creating a multilayer dielectric stack of alternating layers of low-k materials and traditional dielectrics. The more fragile low-k material is ruggedized by a stabilizing layer inserted between layers of low-k films.

Another previous co-assigned United Sales Patent application, SN 60/023,128 disclosed a method and structure for integrating HSQ into mesa isolation structures.

SUMMARY OF THE INVENTION

Respective aspects of the present invention are set forth in claims 1 and 13.

Embodiments of the invention provide an improved method for integrating low dielectric constant materials, which may have undesirable properties such as those discussed above, into integrated circuit structures and processes, especially those requiring multiple levels of interconnect lines.Embodiments of the invention are particularly concerned with improving the mechanical strength and crack resistance of low-k films such as hydrogen silsesquioxane (HSQ).

It has been observed previously that crack formation in HSQ can be affected by factors such as cure temperature, cure ambient, set-time before cure, and film thickness. Some success at crack suppression has been obtained by controlling these conditions. Disclosed herein is a method for further reducing cracks in HSQ by rearranging the process steps of prior art methods to achieve a more robust fabrication process and thicker HSQ layers which are substantially crack free. In general, the process of embodiments of the inventionis to overcoat the HSQ with a permeable and mechanically stable thin film prior to curing.

In a preferred embodiment, interconnect lines are first patterned and etched. A low-k material such as hydrogen

silsesquioxane (HSQ) is spun across the surface of the wafer to fill areas between interconnect lines. The HSQ may be advantageously thicker than achievable in prior art structures. A dielectric stabilizing cap layer such as SiO_2 is then applied on top of the HSQ. The HSQ is then heated on a hot plate to cure. A thick SiO_2 planarization layer may then be applied and planarized. In other embodiments, the HSQ and SiO_2 process steps can be repeated for multiple layers of HSQ.

An advantage of embodiments of the inventionis that no additional process steps are added compared to existing HSQ processes. The process steps are essentially rearranged in sequence, therefore there is no additional costs for the added benefits of the new process.

An additional advantage is high temperature (>450 Celsius) processes can be used subsequent to HSQ application. For example, high temperature furnace cures, such as oxide densification and reflow, are now possible to improve the integrity of the dielectric.

Another advantage is O_2 and H_2O cures can now be used to 'heal' the oxide prior to subsequent processing.

Further, oxygen plasma ashing can now be used with impunity, if needed, since HSQ will be protected from the plasma by the cap layer. Also, the present invention may be combined with the methods of the above referenced applications.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention as well as other features and advantages thereof, will be best understood by reference to the detailed description of illustrative embodiments which follows, read in conjunction with the accompanying drawings, wherein:

FIG. 1 represents a cross-sectional view of a preferred embodiment of the present invention;

FIG. 2a-c show the steps for fabricating the preferred embodiment of Figure 1;

FIG. 3 represents a cross-sectional view of a preferred embodiment of the present invention having multiple levels of interconnect lines; and

FIG. 4 represents a cross-sectional view of another preferred embodiment of the present invention using a caped HSQ layer in trench isolation.

FIG. 5 illustrates an additional embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention are best understood by referring to the drawings, like numerals are used for like and corresponding parts of the various drawings.

With reference to Figure 1, there is shown an embodiment of the present invention, wherein HSQ 18 is deposited between interconnect lines 14 on a semiconductor substrate 10. The HSQ may be applied by one of several methods known in the art and by those listed in the above referenced applications. A thin dielectric cap layer or stabilizing layer 20 covers the HSQ layer. The cap layer may then be followed by additional low-k material layers. The intermetal region may then be completed with a planarized intermetal dielectric layer 22.

With reference to Figures 2a-2c, there is shown a sequence of steps for forming an embodiment of the present invention which is represented by the completed structure shown in Figure 1. Figure 2a illustrates a semiconductor substrate 10 covered with a layer of dielectric 12. The illustrated embodiment of the present invention is directed to reducing capacitance between interconnections on an integrated circuit. Since these interconnections are typically located over the top of active devices fabricated on the surface of a wafer of semiconducting material such as silicon crystal, semiconductor substrate 10 will normally include several layers of various semiconductor materials which make up the active components of the semiconductor device. For simplicity, these layers and devices are not shown in the illustrations. Dielectric layer 12 may be any material suitable for insulating metal interconnect lines 14 from components or other materials in layers below and shown lumped together as semiconductor substrate 10.

Interconnect lines are preferably formed by depositing a layer of aluminum on a preferably planar dielectric layer 12. The aluminum may be masked with a resist, patterned and etched with one of several methods known in the art. This procedure results in the metal connecting lines 14 as shown in figure 2a. The method of an aspect of the invention contemplates using high aspect ratio metal, where the thickness of the interconnect metal is greater than the width. The high aspect ratio interconnects are useful to reduce line resistance while maintaining close spacing for high density circuits. Connection between the interconnects and the circuits below is represented by the via and plug 16. The number and location of vias is determined by the underlying circuit design.

Figure 2b shows HSQ 18 applied between the interconnects 14 on the surface of the wafer. The HSQ 18 is preferably applied by a spin-coat processing in sufficient thickness to fill critical areas between the metal interconnects 14, shown in Figure 2c. The preferred material is poly hydrogen silsesquioxane (HSQ) which has a dielectric constant of less than about 3. This material is manufactured by Dow-Corning, sold under the trade name FOX, and also by Allied Signal, sold under the trade name HSSO. The HSQ is then preferably partially cured at about 300 °C by a hot plate bake on the spin-coater.

The HSQ 18 is followed by a stabilizing cap layer 20 as shown in Figure 2b. The cap layer helps prevent the nucleation and propagation of micro cracks, allows for O_2 and H_2O furnace curing, allows thicker HSQ layers without cracking, and improves planarization. The thickness of the cap layer can be optimized according to the strength and thickness of the HSQ. The cap layer may be dense plasma SiO_2, plasma Si_3N_4, fluorinated SiO_2 or other suitable dielectric. A plasma enhanced chemical vapor deposited SiO_2 cap layer is preferred because it uses the same CF based chemistry for etching as is used for via etch. The thickness of the cap layer is preferably about 1,000 to 3,000 Å, and most preferably about 2,000 Å.

After application of the cap layer 20 the HSQ may be cured. The cap layer helps prevent the nucleation and propagation of micro cracks, allows for O_2 and H_2O furnace curing, allows thicker HSQ layers without cracking, and improves planarization.

The cap layer 20 may then be followed by a thick, about 16,000 Å, SiO_2 interlayer dielectric 22 for planarization. After planarization of the interlayer dielectric, the structure is as shown in Figure 1. In a preferred embodiment, the interlayer dielectric is SiO_2 deposited by plasma enhanced chemical vapor deposition (PECVD) and planarized by chemical mechanical polishing (CMP). As further discussed below, embodiments of the invention combine the advantages of SiO_2 and low dielectric constant materials by placing the low dielectric material between traditional dielectric materials. Structural stability, adhesion, thermal conductivity etc. are enhanced by the SiO_2 or other suitable dielectric.

The method of the present invention may be repeated to form multiple levels of interconnects stacked one upon the other. An example of multiple levels is shown in Figure 3. Typically multiple level interconnects will necessitate vias and contacts 16 from one level to the next. These vias are usually made after the interlevel dielectric has been applied and planarized in a manner well known in the art.

Figure 3 also shows a liner layer 24. The use of a liner layer 24 can be used to keep the HSQ from coming in contact with the interconnects 14. The liner layer may be an etch stopping or protective overcoat layer such as CVD silicon oxide. The HSQ material is then spun onto the surface of tne wafer over the liner layer.

While the structure illustrated in Figure 1 is similar to prior art structures, an important feature should be noted. The method of the present embodiment allows HSQ to be applied to a greater thickness than previously possible. This increased thickness can decrease interconnect capacitance by having more low dielectric constant material between metal interconnect layers, and also decrease fringing capacitance between interconnects on the same metal layer. In prior art structures using prior art methods, the maximum plane field thickness 26 was about 4,000 Å and the maximum HSQ above the interconnect 28 was about 1,000 Å. Using the methods of the prior art, HSQ applied above these maximums had significant cracking problems. An embodiment of the present invention includes a field thickness 26 of greater than 4,000 Å and the HSQ above the interconnect 28 greater than 1,000 Å.

Another embodiment of the present invention is illustrated in Figure 4. This embodiment applies a method embodying the present invention to the structure in US Patent Application S/N 60/023,128. This application discloses a structure wherein HSQ is placed in the isolation trenches to provide a high temperature resistant trench refill. It was discovered that applying a cap layer to the HSQ prior to furnace cure is also beneficial in this structure. Specifically, the cap layer allows thicker HSQ layers without deleterious effects, increasing the possible layer thickness above 1μm. A cap layer also allows for O_2 and H_2O furnace curing of the HSQ and reduces shrinkage of the HSQ layer.

As illustrated in Figure 4, a silicon substrate 10 has an isolation trench 30 to isolate adjacent active devices such as transistors 32. The nitride cap 22 is both a hardmask for trench formation etch and a CMP stop for oxide planarization. The surface of the substrate is preferably then spin-coated with HSQ 18. The HSQ 18 is then preferably partially cured by a hot plate bake on the spin-coater. A capping layer 20, preferably PETEOS, is applied as discussed above. After the capping layer is applied, the HSQ can be safely furnace cured at 1050 °C in N_2, O_2 or at 850 °C in H_2O. The furnace cure is preferably for 15 to 100 minutes and most preferably for about 30 minutes.

An additional embodiment of the present invention is illustrated in Figure 5. This embodiment uses an HSQ layer for a poly metal dielectric layer. As illustrated in Figure 5, a silicon substrate 10 has one or more gates 34. The gates may include isolation trenches 30 to isolate adjacent active devices. The surface of the substrate is preferably spin-coated with HSQ 18. The HSQ 18 is then preferably partially cured by a hot plate bake on the spin-coater. A capping layer 20, preferably PETEOS, is applied as discussed above. After the capping layer is applied, the HSQ can be safely furnace cured at 1050 °C in N_2, O_2 or at 850 °C in H_2O. The furnace cure is preferably for 15 to 100 minutes and most preferably for about 30 minutes. This embodiment may be used in combination with the other embodiments described above.

The present invention also contemplates using a stabilizing layer in combination with the structures and techniques

disclosed in the previous co-assigned applications listed above.

The sole Table, below, provides an overview of some embodiments and the drawings.

Table I

Drawing Element	Preferred or Specific Examples	Generic Term	Other Alternate Examples
10	Silicon Substrate	Substrate or Wafer	GaAs
12	Silicon Oxide	Buffer Layer	
14	Aluminum	Interconnect Line	TiN/Al/TiN, Cu, W
16	Tungsten	Via	Aluminum
18	HSQ	Low Dielectric Constant Material	Xerogel, organic SOGs, low dielectric constant polymers
20	TEOS	Capping Layer	Fluorinated SiO_2, Si_3N_4, Diamond, or other dielectrics with good mechanical strength.
22	SiO_2	Inter-metal Dielectric	Fluorinated SiO_2, Si_3N_4, Diamond, or other dielectrics with good mechanical strength.
24	Silicon Oxide	Liner	Fluorinated SiO_2
30	Trench		
32	Nitride	Polishing Stop	
34	Silicon Oxide	Pad Oxide	

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description.

Claims

1. A method of forming a microelectronic structure, said method comprising:

applying a layer of hydrogen silsesquioxane over a substrate;
applying a capping layer to said hydrogen silsesquioxane layer;
curing the hydrogen silsesquioxane layer.

2. The method according to Claim 1, further comprising: applying said hydrogen silsesquioxane between interconnect lines on said substrate.

3. The method according to Claim 1 or Claim 2, further comprising the additional step of providing a liner layer over said conductive interconnect lines prior to said step of applying said hydrogen silsesquioxane.

4. The method according to any preceding claim, further comprising applying said hydrogen silsesquioxane in isolation trenches on said substrate.

5. The method according to any preceding claim, further comprising selecting said capping layer from a group of material comprising: SiO_2 and S_3N_4, and fluorinated SiO_2.

6. The method according to any preceding claim, wherein curing step comprises curing in an ambient selected from the group comprising: C_xH_y, C_xF_y, N_2, O_2, H_2O and Forming Gas (mixture of H_2 and N_2).

7. The method according to any preceding claim, further comprising performing said curing step at a temperature above approximately 400 °C.

8. The method according to any preceding claim, further comprising performing said curing step at a temperature above 800°C.

9. The method according to any preceding claim, further comprising the step of planarizing said second dielectric subsequent to deposition and then repeating the steps of applying the layer of hydrogen silsesquioxane, applying a capping layer, and curing the hydrogen silsesquioxane to create a multilevel interconnect structure.

10. The method according to any preceding claim further comprising providing a semiconductor substrate having metal interconnects;

and wherein the step of applying the layer of hydrogen silsesquioxane on said substrate further comprises applying the layer of hydrogen silsesquioxane over said interconnects;

11. The method according to Claim 10, further comprising applying said hydrogen silsesquioxane between interconnect lines on said substrate.

12. The method according to Claim 10 or Claim 11, further comprising the step of providing a liner layer over said conductive interconnect lines prior to applying said hydrogen silsesquioxane.

13. A microelectronic device structure comprising:

a layer of hydrogen silsesquioxane formed on a substrate:
a capping layer formed on said hyrdogen silsesquioxane layer: and
wherein said hydrogen silsesquioxane layer forms a substantially crack free cured layer having a thickness greater than approximately 4000 Å

14. The structure according to Claim 13, wherein said hydrogen silsesquioxane is applied between interconnect lines on said substrate.

15. The structure according to Claim 13 or Claim 14, wherein said hydrogen silsesquioxane is applied in isolation trenches on said substrate.

16. The structure according to any of Claims 13 to 15, wherein said capping layer is chosen from the group of SiO_2 and S_3N_4, and fluorinated SiO_2.

17. The structure according to any of Claims 13 to 16, wherein said hydrogen silsesquioxane is applied over device gates as a poly-metal dielectric on said semiconductor substrate.

FIG. 1

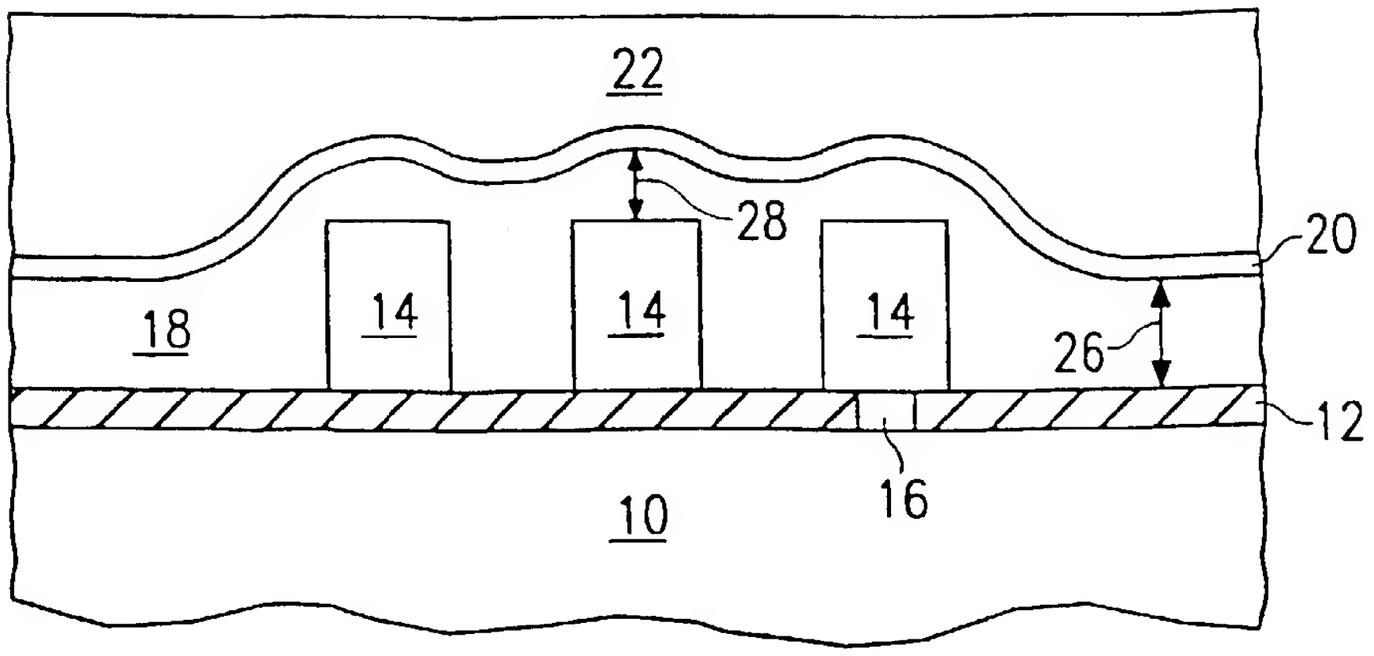

FIG. 2a

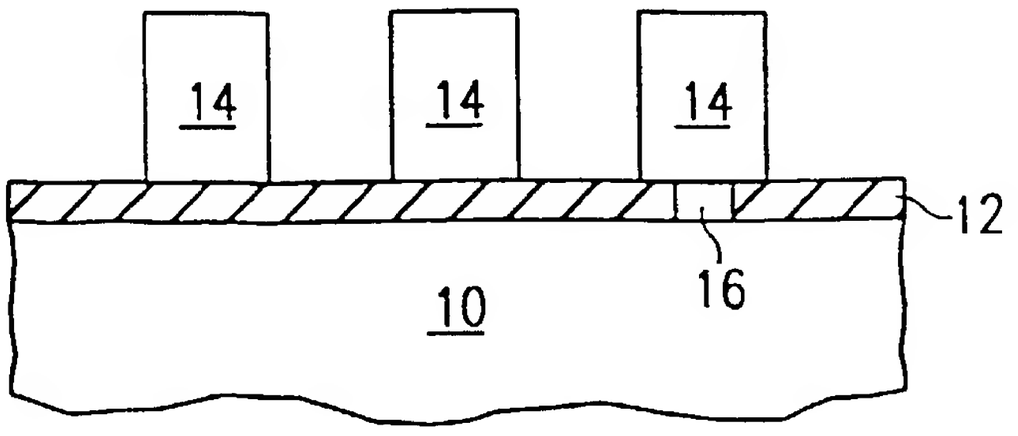

FIG. 2b

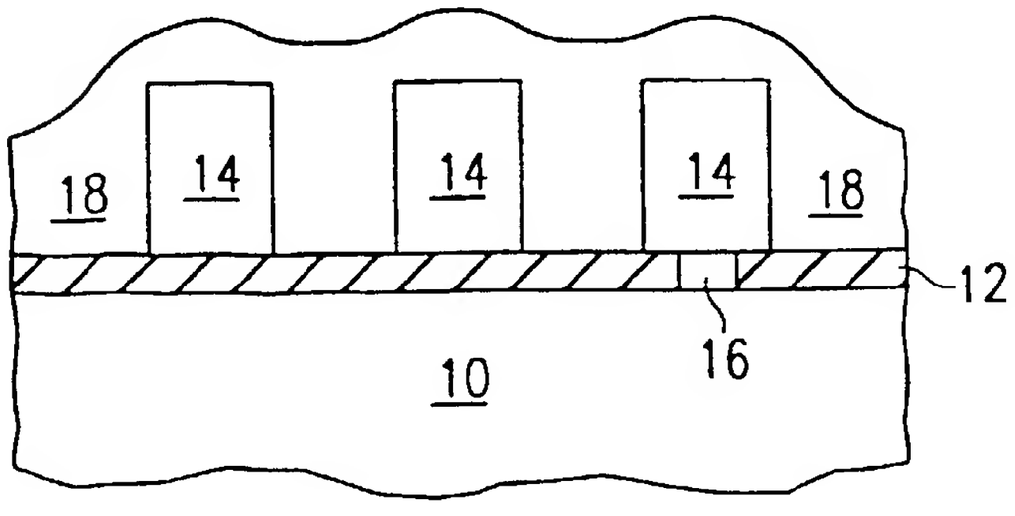

FIG. 2c

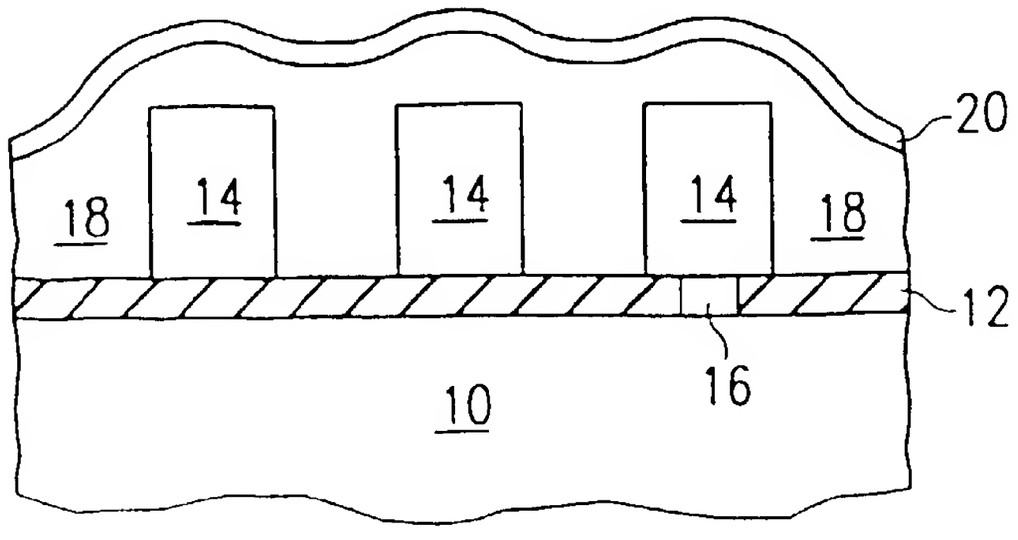

FIG. 3

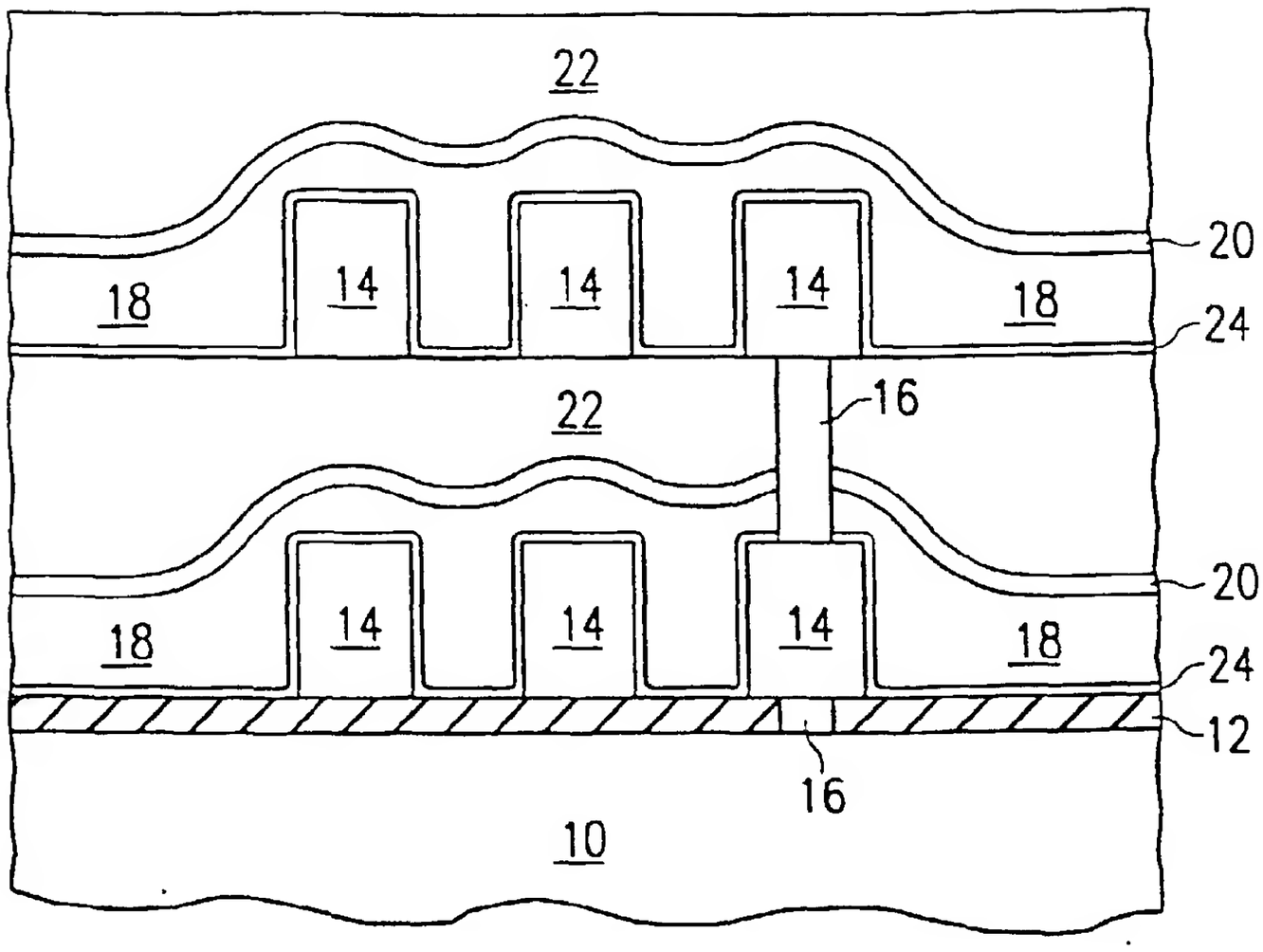

FIG. 4

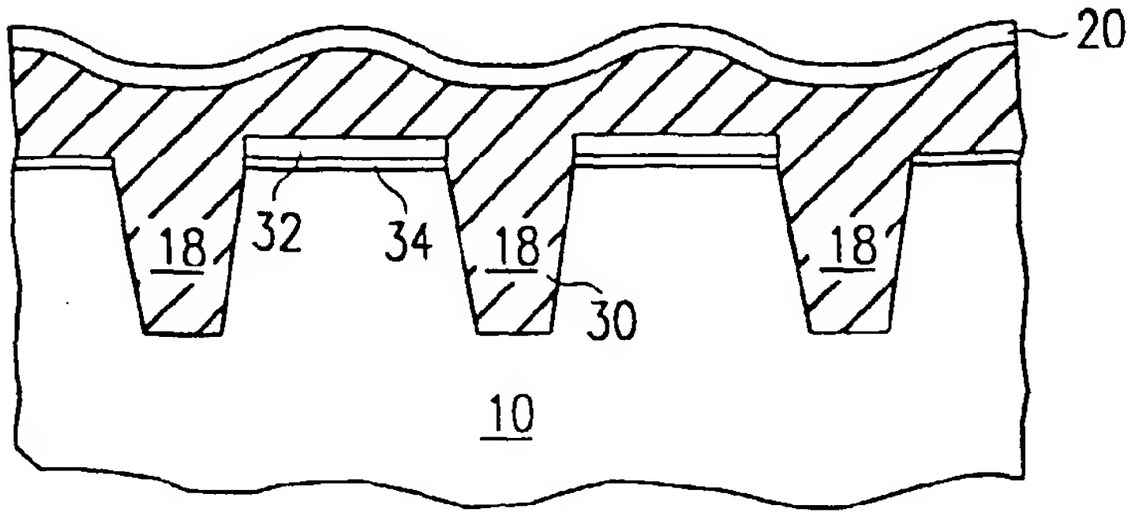

FIG. 5